AMENDMENTS TO THE CLAIMS:

Claim 1. (currently amended) A method for providing context save and restore using a test scan chain in an integrated circuit device ~~multi-channel functionality with a telecommunication device comprising a single channel~~, the method comprising:

dividing a scan chain of digital logic components into a plurality of sub-chains;

providing a first data set in the sub-chains;

linking the sub-chains in parallel and to a hardware resource for executing an application;

linking the sub-chains to a device memory;

executing a first application to update the first data set in the sub-chains, the first application operable to use the hardware resource ~~channel~~;

storing the updated first data set in the device memory;

restoring a second data set from the device memory to the sub-chains; and

executing a second application to update the second data set in the sub-chains, the second application being operable to use the hardware resource ~~channel~~, the device being operable to be placed in a test mode for testing, a functional mode for executing applications, and a switch mode for switching between applications, each digital logic component operable to receive test data over a test line and a test clock signal while the device is in the test mode, to receive functional data over a functional line and a functional clock signal while the device is in the functional mode, and to receive functional data over the functional line and the functional clock signal while the device is in the switch mode.

Claim 2. (original) The method of Claim 1, the device memory comprising a write port and a read port, storing the updated first data set in the device memory comprising shifting the updated first data set to the device memory through the write port, and restoring the second data set from the device memory to the sub-chains comprising shifting the second data set from the device memory through the read port to the sub-chains.

Claim 3 (canceled)

Claim 4. (currently amended) The method of Claim 1 ~~3~~, storing the updated first data set comprising storing the updated first data set while the device is in the switch mode, and restoring the second data set comprising restoring the second data set while the device is in the switch mode.

Claim 5. (currently amended) The method of Claim 1, further comprising:

storing the updated second data set in the device memory;

restoring a third data set from the device memory to the sub-chains;

executing a third application to update the third data set in the sub-chains, the third application operable to use the hardware resource ~~channel~~;

storing the updated third data set in the device memory;

restoring a fourth data set from the device memory to the sub-chains;

executing a fourth application to update the fourth data set in the sub-chains, the fourth application operable to use the hardware resource ~~channel~~;

storing the updated fourth data set in the device memory; and

restoring the first data set from the device memory to the sub-chains.

Claim 6. (original) The method of Claim 1, the device comprising one of an application-specific integrated circuit and a field-programmable gate array.

Claim 7. (original) The method of Claim 1, each digital logic component comprising a flip-flop.

Claim 8. (currently amended) The method of Claim 1, wherein the step of dividing the scan chain of digital logic components into a plurality of sub-chains comprises ~~comprising~~ dividing the scan chain into a specified number of sub-chains, the specified number corresponding to a data width for the device memory.

Claim 9. (currently amended) A method for providing context save and restore using a test scan chain in an integrated circuit device ~~multi-channel functionality with a telecommunication device comprising a single channel~~, the method comprising:

linking a plurality of sub-chains of digital logic components in parallel and to a hardware resource for executing an application;

linking the sub-chains to a write port of a device memory and to a read port of the device memory;

providing a first data set in the sub-chains;

executing a first application to update the first data set in the sub-chains, the first application operable to use the hardware resource ~~channel~~;

shifting the updated first data set into the device memory through the write port;

shifting a second data set from the device memory through the read port into the sub-chains; and

executing a second application to update the second data set in the sub-chains, the second application being operable to use the hardware resource ~~channel~~, the device operable to be placed in a test mode for testing, a functional mode for executing applications, and a switch mode for switching between applications, each digital logic component operable to receive test data over a test line and a test clock signal while the device is in the test mode, to receive functional data over a functional line and a functional clock signal while the device is in the functional mode, and to receive functional data over the functional line and the functional clock signal while the device is in the switch mode.

Claim 10 (canceled)

Claim 11. (currently amended) The method of Claim 9 ~~10~~, wherein the step of shifting the updated first data set into the device memory through the write port comprises ~~comprising~~ shifting the updated first data set into the device memory while the device is in the switch mode, and shifting the second data set from the device memory through the read port into the sub-chains comprising shifting the second data set from the device memory while the device is in the switch mode.

Claim 12. (currently amended) The method of Claim 9, further comprising:

shifting the updated second data set into the device memory through the write port;

shifting a third data set from the device memory through the read port into the sub-chains;

executing a third application to update the third data set in the sub-chains, the third application operable to use the hardware resource ~~channel~~;

shifting the updated third data set into the device memory through the write port;

shifting a fourth data set from the device memory through the read port into the sub-chains;

executing a fourth application to update the fourth data set in the sub-chains, the fourth application operable to use the hardware resource ~~channel~~;

shifting the updated fourth data set into the device memory through the write port; and

shifting the first data set from the device memory through the read port into the sub-chains.

Claim 13. (original) The method of Claim 9, the device comprising one of an application-specific integrated circuit and a field-programmable gate array.

Claim 14. (original) The method of Claim 9, each digital logic component comprising a flip-flop.

Claim 15. (currently amended) The method of Claim 9, wherein the step of dividing the scan chain of digital logic components into a plurality of sub-chains comprises ~~comprising~~ dividing the scan chain into a specified number of sub-chains, the specified number corresponding to a data width for the device memory.

Claim 16. (currently amended) A processing ~~telecommunication~~ device ~~comprising a single channel~~, ~~the device~~ comprising:

a scan chain comprising a plurality of digital logic components;

a hardware resource for executing an application;

a device memory operable to store a data set for each of a plurality of applications; and

a state machine operable to divide the scan chain into a plurality of sub-chains, to provide a first data set in the sub-chains, to link the sub-chains in parallel and to the hardware resource, to link the sub-chains to the device memory, to execute a first application to update the first data set in the sub-chains, the first application operable to use the hardware resource ~~channel~~, to shift the updated first data set into the device memory for storage, to shift a second data set from the device memory into the sub-chains, and to execute a second application to update the second data set in the sub-chains, the second application operable to use the hardware resource ~~channel~~, the state machine further operable to place the device in a test mode for testing, a functional mode for executing applications, and a switch mode for switching between applications, each digital logic component operable to receive test data over a test line and a test clock signal while the device is in the test mode, to receive functional data over a functional line and a functional clock signal while the device is in the functional mode, and to receive functional data over the functional line and the functional clock signal while the device is in the switch mode.

Claim 17. (original) The device of Claim 16, each digital logic component comprising a flip-flop.

Claim 18. (original) The device of Claim 16, the state machine further operable to divide the scan chain into a specified number of sub-chains, the specified number corresponding to a data width for the device memory.

Claim 19 (canceled)

Claim 20. (currently amended) The device of Claim 16 ~~19~~, the state machine further operable to shift the updated first data set into the device memory while the device is in the switch mode, and to shift the second data set from the device memory into the sub-chains while the device is in the switch mode.